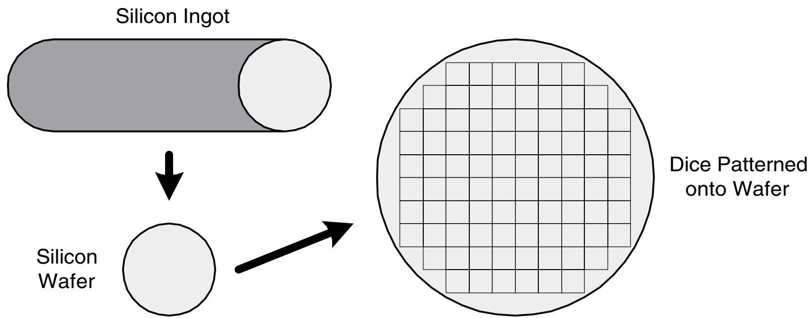

FIGURE 2.3 Silicon wafer.

When the paper is developed in a chemical bath, portions of the paper that were exposed change color and yield a visible image.

Photographic processes provide excellent resolution of detail. Engineers apply this same principle in fabricating ICs to create details that are fractions of a micron in size. Similar to a photographic negative, a mask is created for each IC processing step. Like a photographic negative, the mask does not have to be the same size as the silicon area it is to expose because, with lenses, light can be focused through the mask to an arbitrary area. Using a technique called *photolithography,* the silicon surface is first prepared with a light-sensitive chemical called *photoresist*. The prepared surface is then exposed to light through the mask. Depending on whether a positive or negative photoresist process is employed, the areas of photoresist that have been either exposed or not exposed to light are washed away in a chemical bath, resulting in a pattern of bare and covered areas of silicon. The wafer can then be exposed to chemical baths, high temperature metal vapors, and ion beams. Only the bare areas that have had photoresist washed away are affected in this step. In this way, specific areas of the silicon wafer can be doped according to the IC designers' specifications. Successive mask layers and process steps can continue to wash away and expose new layers of photoresist and then build sandwiches of semiconductor and metal material. A very simplified view of these process steps is shown in Fig. 2.4. The semiconductor fabrication process must be performed in a clean-room environment to prevent minute dust particles and other contaminants from disturbing the lithography and chemical processing steps.

In reality, dozens of such steps are necessary to fabricate an IC. The semiconductor structures that must be formed by layering different metals and dopants are complex and must be formed one thin layer at a time. Modern ICs typically have more than four layers of metal, each layer separated from others by a thin insulating layer of silicon dioxide. The use of more metal layers increases the cost of an IC, but it also increases its density, because more metal wires can be fabricated to connect more transistors. This complete process from start to finish usually takes one to four weeks. The chemical diffusion step (5) is an example of how different regions of the silicon wafer are doped to achieve varying electrical characteristics. In reality, several successive doping steps are required to create transistors. The metal deposition step (10) is an example of how the microscopic metal wires that connect the many individual transistors are created. Hot metal vapors are passed over the prepared surface of the wafer. Over time, individual molecules adhere to the exposed areas and form continuous wires. Historically, most metal interconnects on silicon ICs are made from aluminum. However, copper has become a common component of leading-edge ICs.

As IC feature sizes continue to shrink, the physical properties of light can become limiting factors in the resolution with which a wafer can be processed. Shorter light wavelengths are necessary to

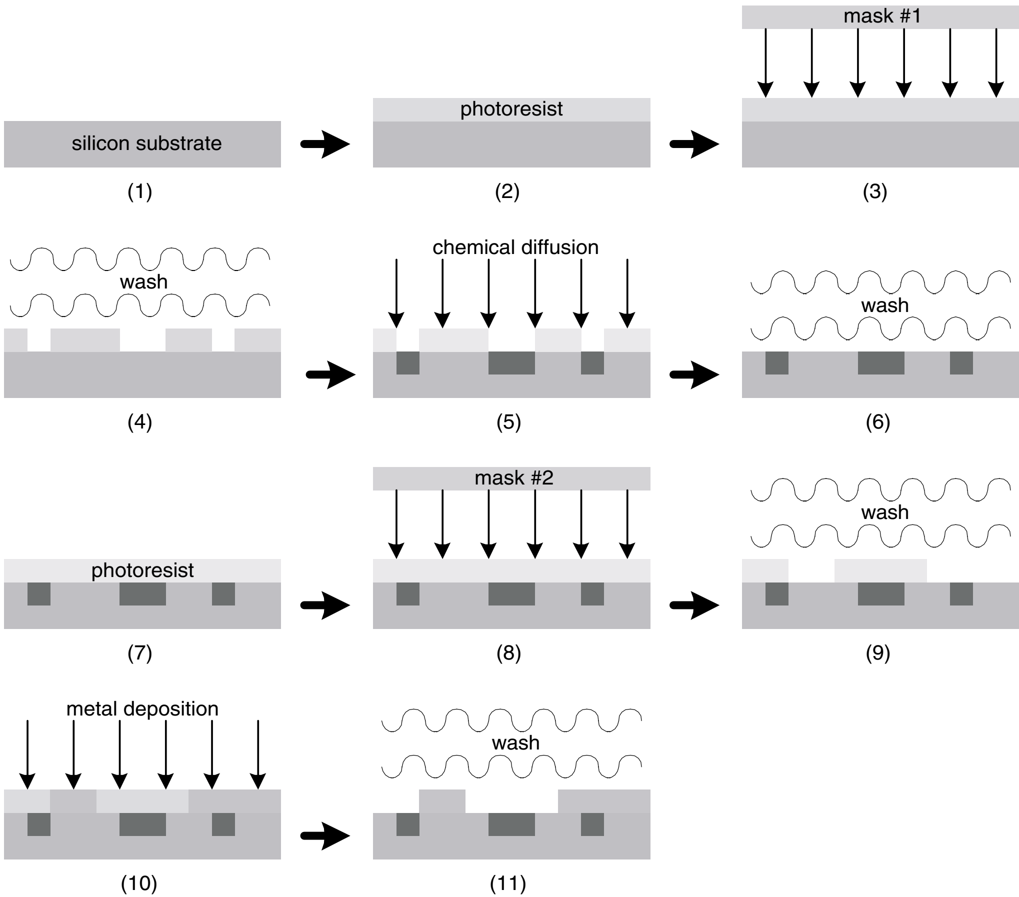

FIGURE 2.4 The IC fabrication process.

meet the demands of leading-edge IC process technology. The human eye can detect electromagnetic energy from about 700 nm (red) to 400 nm (violet). Whereas ultraviolet light (< 400 nm) was once adequate for IC fabrication, deep UV wavelengths are now in use, and shorter wavelengths below 200 nm are being explored.

Each of the process steps is applied to the entire wafer. The many dice on a single wafer are usually exposed to light through the same mask. The mask is either large enough to cover the entire wafer and therefore expose all dice at once, or the mask is stepped through the dice grid (using a machine appropriately called a *stepper*) such that each die location is exposed separately before the next processing step. In certain cases, such as small-volume or experimental runs, different die locations on the same wafer will be exposed with different masks. This is entirely feasible but may not be as efficient as creating a wafer on which all dice are identical.

When an IC is designed and fabricated, it generally follows one of two main transistor technologies: bipolar or metal-oxide semiconductor (MOS). Bipolar processes create BJTs, whereas MOS processes create FETs. Bipolar logic was more common before the 1980s, but MOS technologies